

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0004] with the following amended paragraph:

[0004] Fig. 1 is a block diagram showing a related pilot signal searcher. As shown in Fig. 1, a searcher 100 includes a PN (pseudo noise) code generator 1, a despreading device 2, a coherent accumulator 3, an energy calculator 5, a non-coherent accumulator 6, and a sorter 8. An input signal received through an antenna (not shown) is input into the despreading device 2 after being separated into an I (in-phase) component and a Q (quadrature) component. When the I and Q component input signals are both input into the despreading device 2, the PN code generator 1 creates corresponding I and Q PN codes for input into the despreading device 2. The PN code generator 1 generates the PN codes corresponding to one PN offset. The I and Q component input signals are input into the despreading device 2 as many as the number determined at the coherent accumulator 3 and the non-coherent accumulator 6. The despreading device 2 despreads the received input signals by using the inputted PN codes and transmits output signals into the coherent accumulator 3. ~~In output signal~~ Output signals from the despreading device 2 are the I and Q components. That is to say, the despreading device 2 despreads the first input signal by using relevant first PN code among the PN codes, and then despreads the second input signals that are input after the first input signal using the next relevant PN code. The above-described operations are repeated according to the number of input signals determined by the coherent accumulator 3 and the non-coherent accumulator 6.

Please replace paragraph [0027] with the following amended paragraph:

[0027] Fig. 3 is a block diagram illustrating a preferred embodiment of an apparatus for signal search according to the present invention. As shown in Fig. 3, the preferred embodiment of an apparatus will be described for pilot signal search performing coherent accumulation in the unit of 32

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PN chips and searches in the resolution of $\frac{1}{2}$ PN chip. However, the present invention is not intended to be so limited. As shown in Fig. 3, a pilot signal searcher 300 includes a first shift register bank 32 for sequentially storing PN codes, a second shift register bank 33 for sequentially storing input signals, and a despreader 50 can include a plurality of despreading circuits for despreading in parallel the input signals using the PN code. A coherent accumulator 34 is for accumulating the despreaded signals outputted from the despreading circuit 50, and a buffer 35 is for storing temporarily accumulation signals from the coherent accumulator 34 accumulated when the accumulation length of a coherent accumulator 34 is a plurality of the coherent accumulation unit, which is 32 PN chips in this example of the preferred embodiment of an apparatus for signal search.

Please replace paragraph [0029] with the following amended paragraph:

[0029] The first shift register bank 32, the second shift register bank 33, the despreading circuit 50, and the coherent accumulator ~~[[43]]~~ 34 will now be described in more detail. Fig. 4 is a block diagram illustrating a configuration including the despreading circuit 50 and the coherent accumulator 34 as shown in Fig. 3.

Please replace paragraph [0042] with the following amended paragraph:

[[0042] A case where the length of the coherent accumulation is a plurality of the coherent accumulation unit, which is 32 as shown in Fig. 4, will now be described. In this case, the second adder 55e and 55f and a buffer 35 can be used. For example, the length of the coherent accumulation is 64 and will be called the first despreading signal and the second despreading signal. The despreaded results from the first despreading unit 52 and the second despreading unit 53 can include 32 pieces of the despreaded results having I and Q components, respectively. However, the first despreaded result outputted from the first despreading unit 52 and the second despreading unit 53 is respectively

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accumulated by the first adder 55a, 55b[[j]], 55c, 55d, and the outputted accumulation signal is temporarily stored in the buffer 35. The storing of the temporal coherent accumulation results is performed for other PN offsets by shifting the second shift register bank 33 while the contents of the first shift register bank 32 is maintained. After storing the temporal coherent accumulation results for all possible PN offsets, the next 32 PN codes following the PN codes used above are loaded to the first shift register bank 32, and the same process is performed as described above. At this time, the second ~~adder-adders~~ 55e, 55f, 55g and 55g are used to add the current coherent accumulation results and the temporal coherent accumulation results stored in buffer 35. The same process is applied to all the possible PN offsets. After finishing the coherent accumulation for all possible PN offsets, the energy calculation and the non-coherent accumulation for all possible PN offsets are performed. Such operation processes for this example can be as shown in Fig. 5. Accordingly, preferred embodiments of the signal searcher can be used to increase the length of coherent calculation.